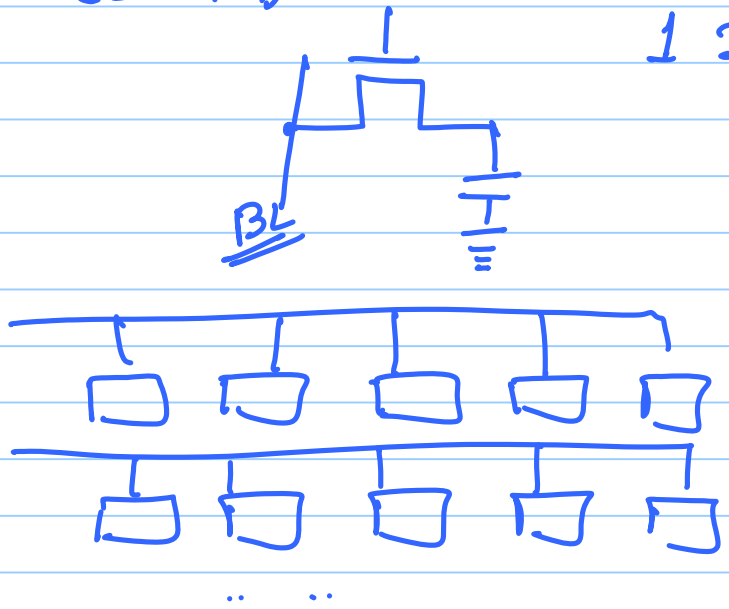
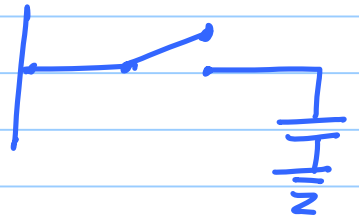
Sept -14

Note Title 14-09-2011

Dynamic RAM (DRAM)



1 DRAM cell.



Periodic Refresh

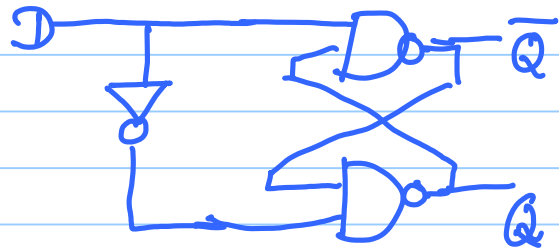
SRAM	DRAM	LATCH
+ fast	- slow	++ very fast
+ dense	++ very dense	- bad

+- moderate power
- 6 Trans.

+ very power efficient.
+ (1 Trans + Icap)

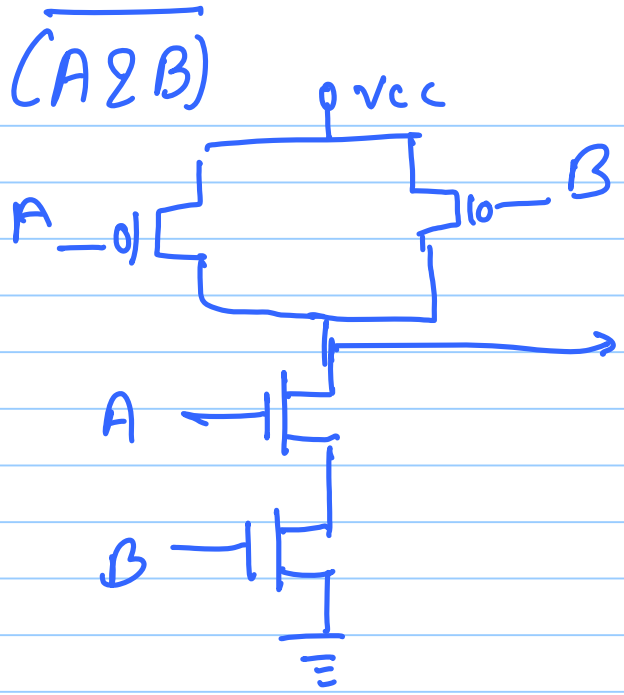
- very bad
- bad (18 T)

D Flip-Flop.

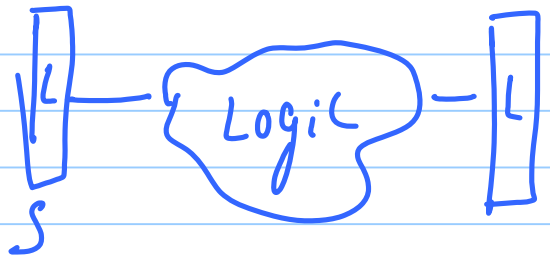


(10 T)

NAND GATE $\overline{(A \cdot B)}$



Logic



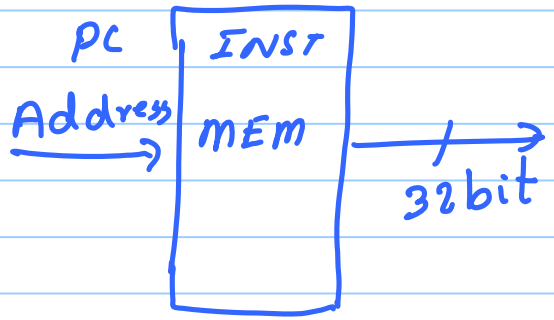
Adder
Subtracter
=
=

M
- SRAM
- DRAM
- LATCH

L
Logic Gates.
(OR, NOT, NAND, ---)

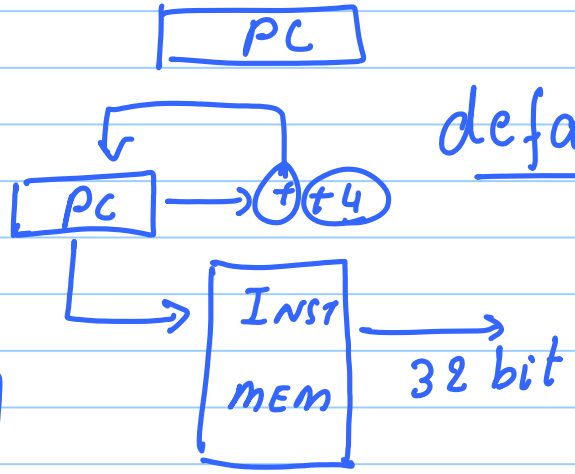
Pipeline

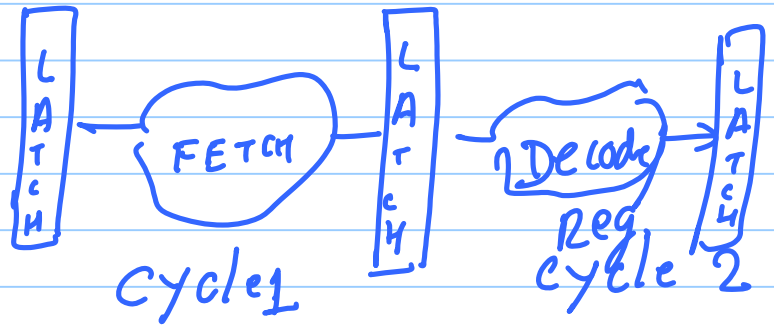
1st Stage : Fetch



3 state

default.



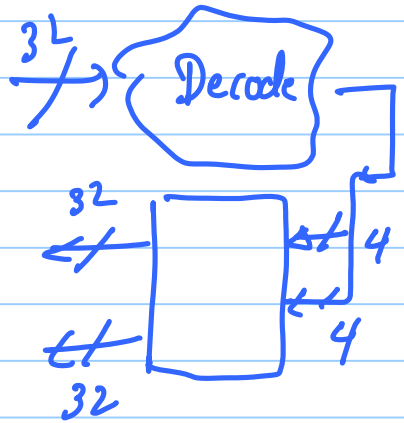


Stage 2.

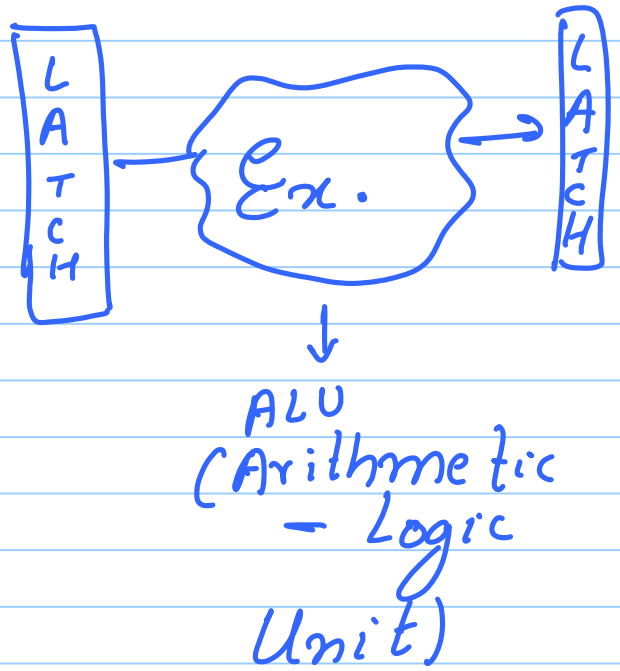
a) Decode the 32 bits.

- Type
- Registers
- Expand immediates.

b) Register Access (read values)



Stage 3. Execute.

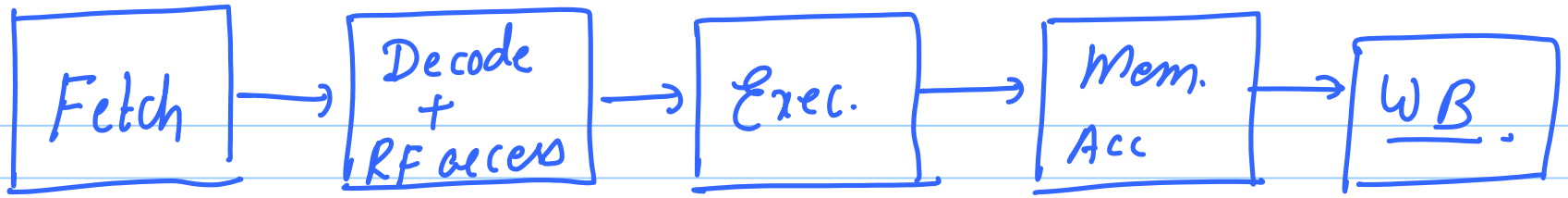


Stage 4 Memory Access.

(address, value (store))

Stage 5. Writeback.

Write the result back to the register file.



(5 stage Pipeline).

TODO:

1) Take a look at chapter 4

2) Read the MIPS ISA

3) Understand the MIPS Instruction Format.